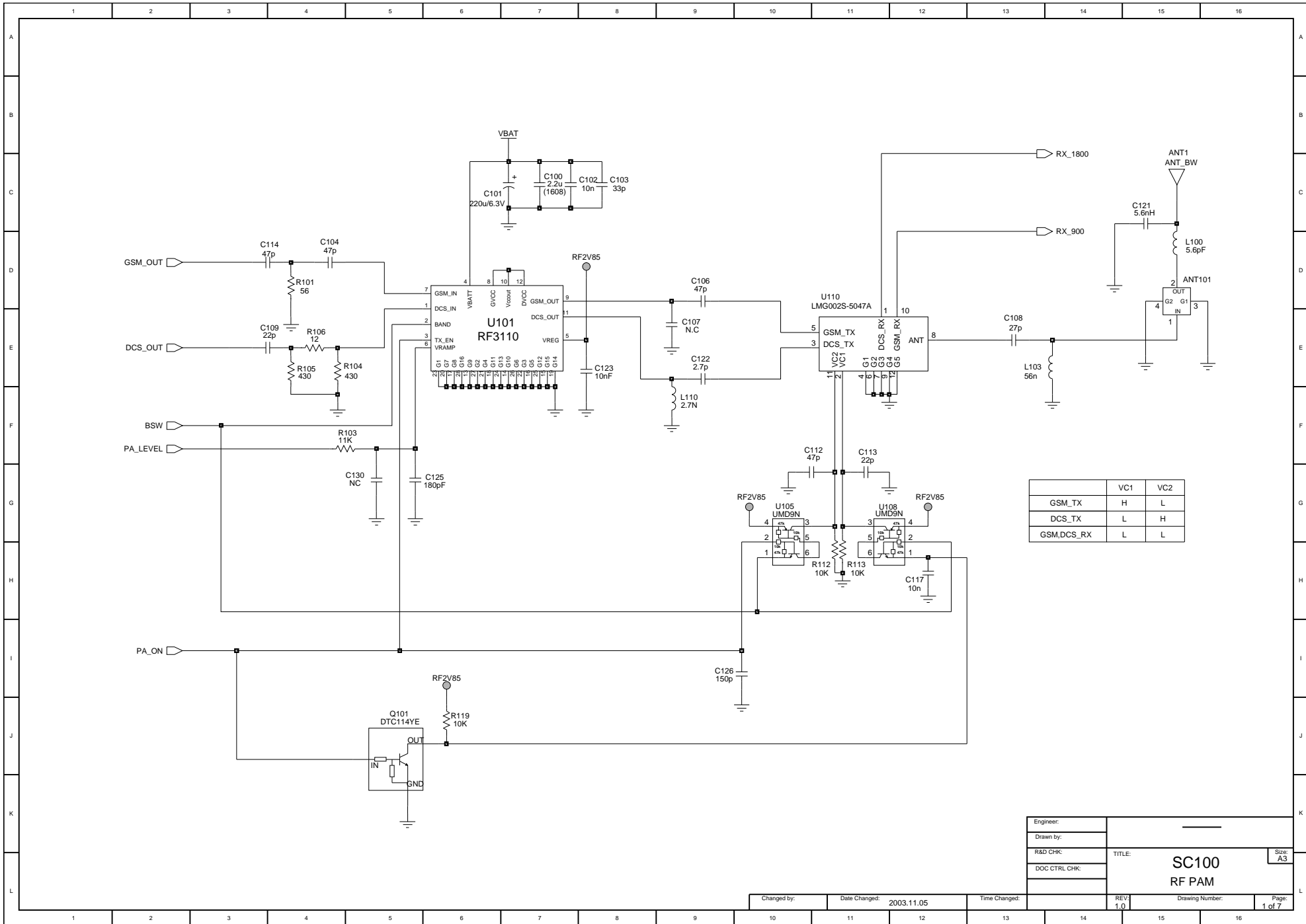


7.1 RF PAM

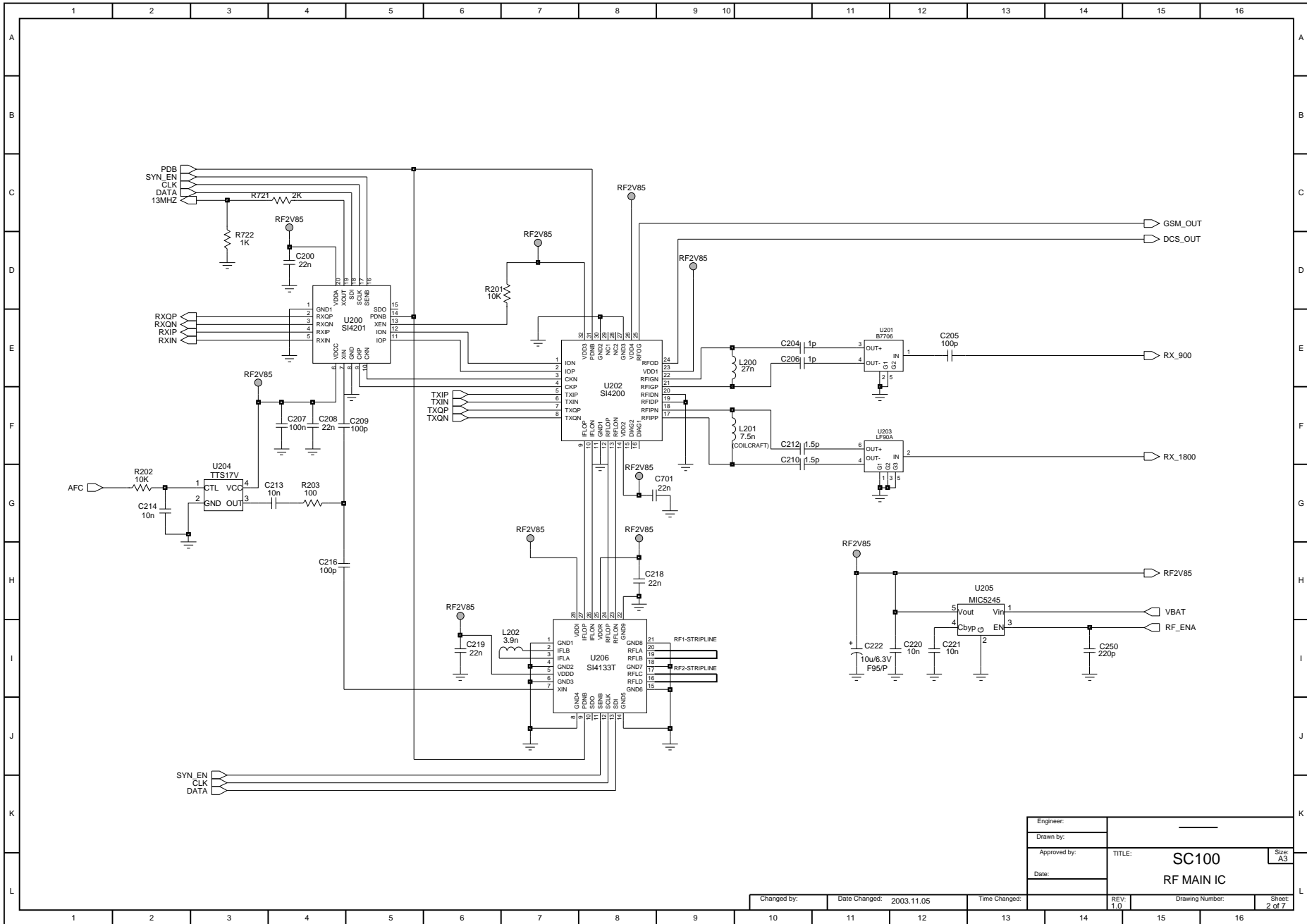


	VC1	VC2
GSM_TX	H	L
DCS_TX	L	H
GSM_DCS_RX	L	L

Engineer:	
Drawn by:	
R&D CHK:	TITLE: SC100
DOC CTRL CHK:	RF PAM
Size: A3	

Changed by:	Date Changed: 2003.11.05	Time Changed:	REV: 1.0	Drawing Number:	Page: 1 of 7
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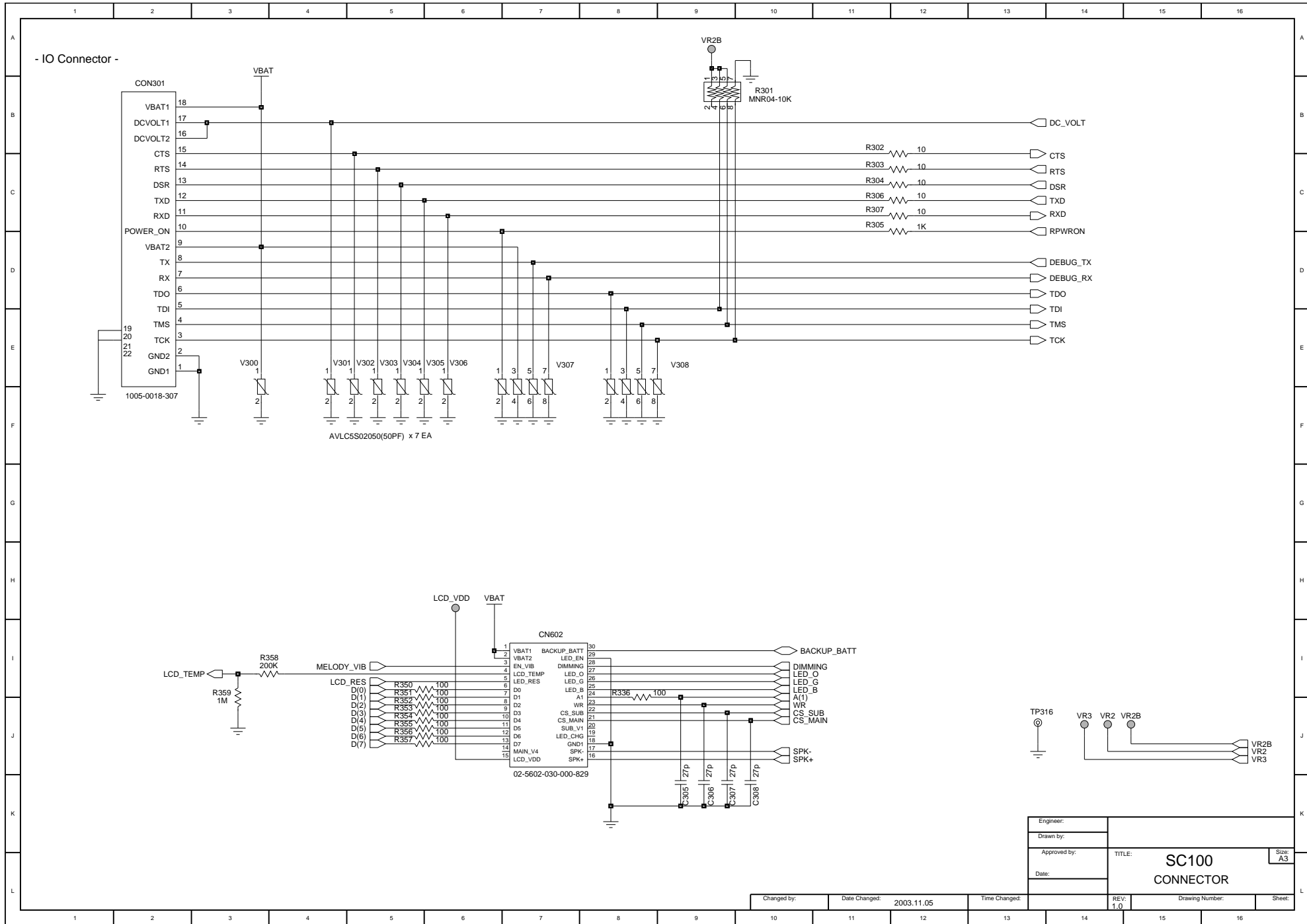
7.2 RF Main Chip



Engineer:			
Drawn by:			
Approved by:	TITLE:	SC100	Size: A3
Date:	RF MAIN IC		

Changed by:	Date Changed:	2003.11.05	Time Changed:	REV:	1.0	Drawing Number:	Sheet:	2 of 7
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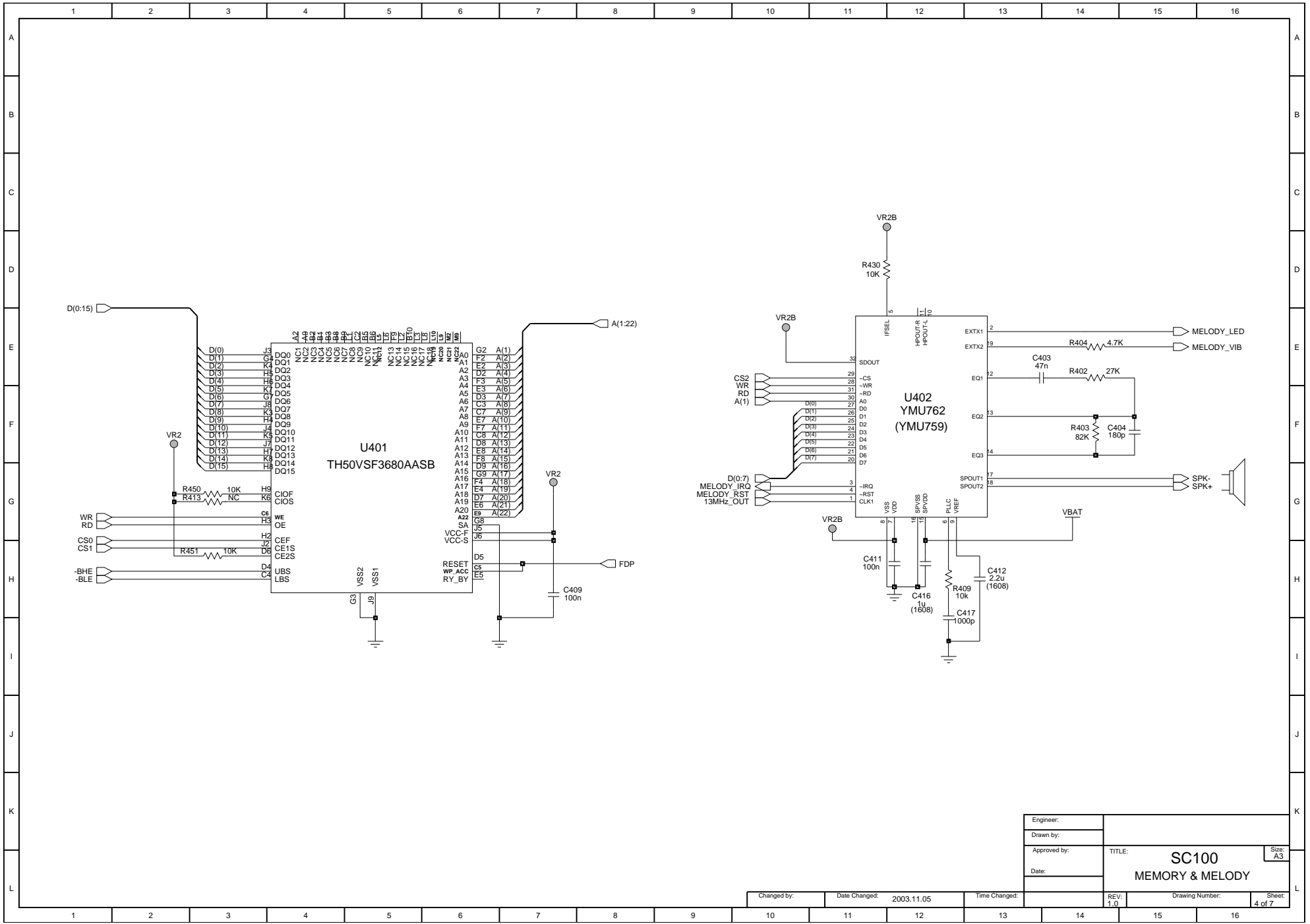
7.3 Connectors



Engineer:	
Drawn by:	
Approved by:	TITLE: SC100
Date:	Size: A3
CONNECTOR	

Changed by:	Date Changed: 2003.11.05	Time Changed:	REV: 1.0	Drawing Number:	Sheet:
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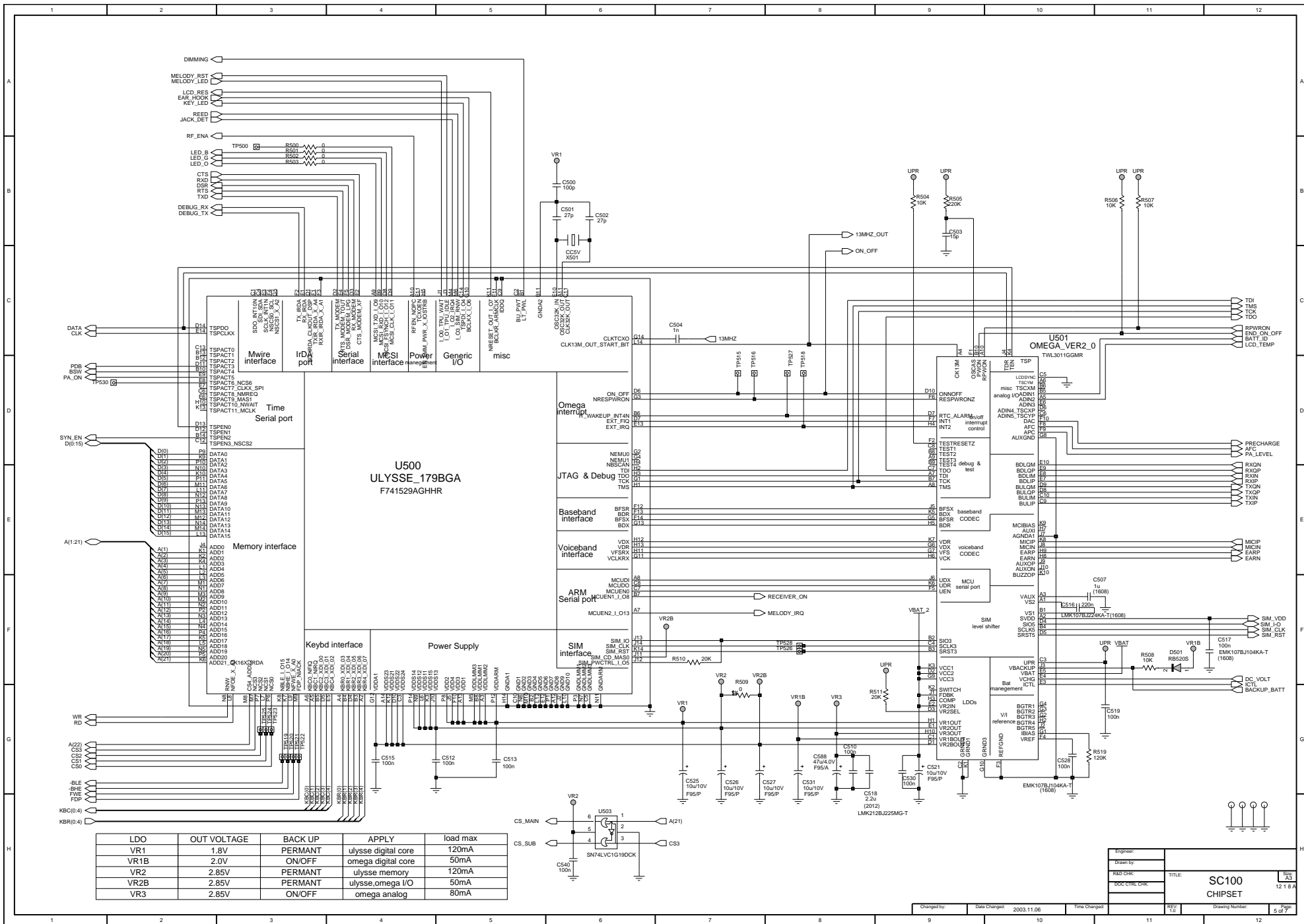
7.4 Memory & Melody



Engineer:	
Drawn by:	
Approved by:	TITLE: SC100
Date:	Size: A3
MEMORY & MELODY	

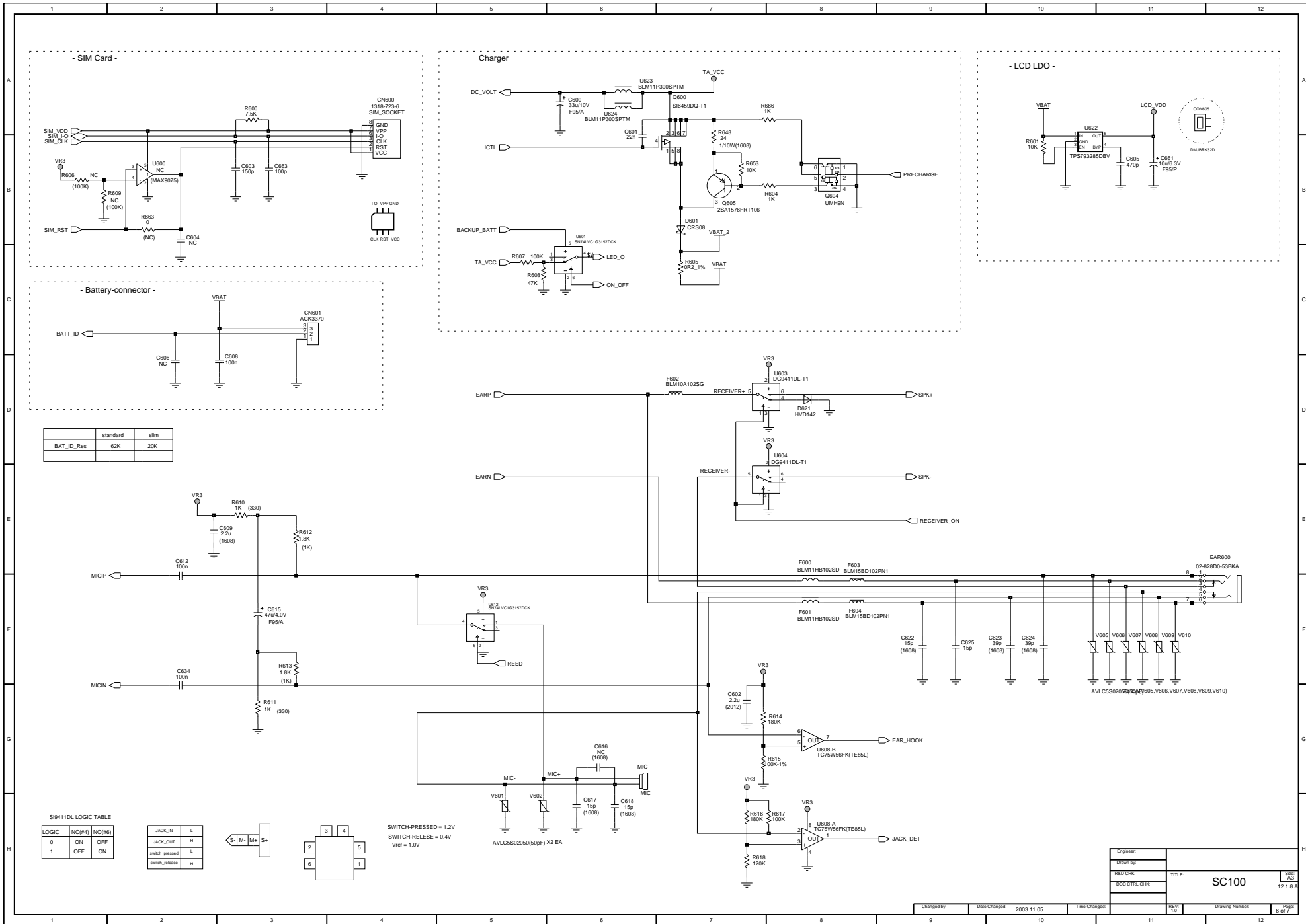
Changed by:	Date Changed: 2003.11.05	Time Changed:	REV: 1.0	Drawing Number:	Sheet: 4 of 7
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7.5 Main Chip(Ulyesse/Omega)



Engineer:		Rev:	A3
Drawn by:		TITLE:	SC100
Field OK:		DATE:	12 18 A
VOC-CTRL CLK:		Drawing Number:	5 of 5
Charged by:		Date Changed:	2003.11.06
Time Changed:			

7.6 Audio & SIM connector

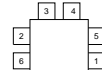


	standard	slim
BAT_ID_Res	62K	20K

SB941DL LOGIC TABLE

LOGIC	NC(41)	NO(98)
0	ON	OFF
1	OFF	ON

JACK_IN	L
JACK_OUT	H
switch_pressed	L
switch_release	H

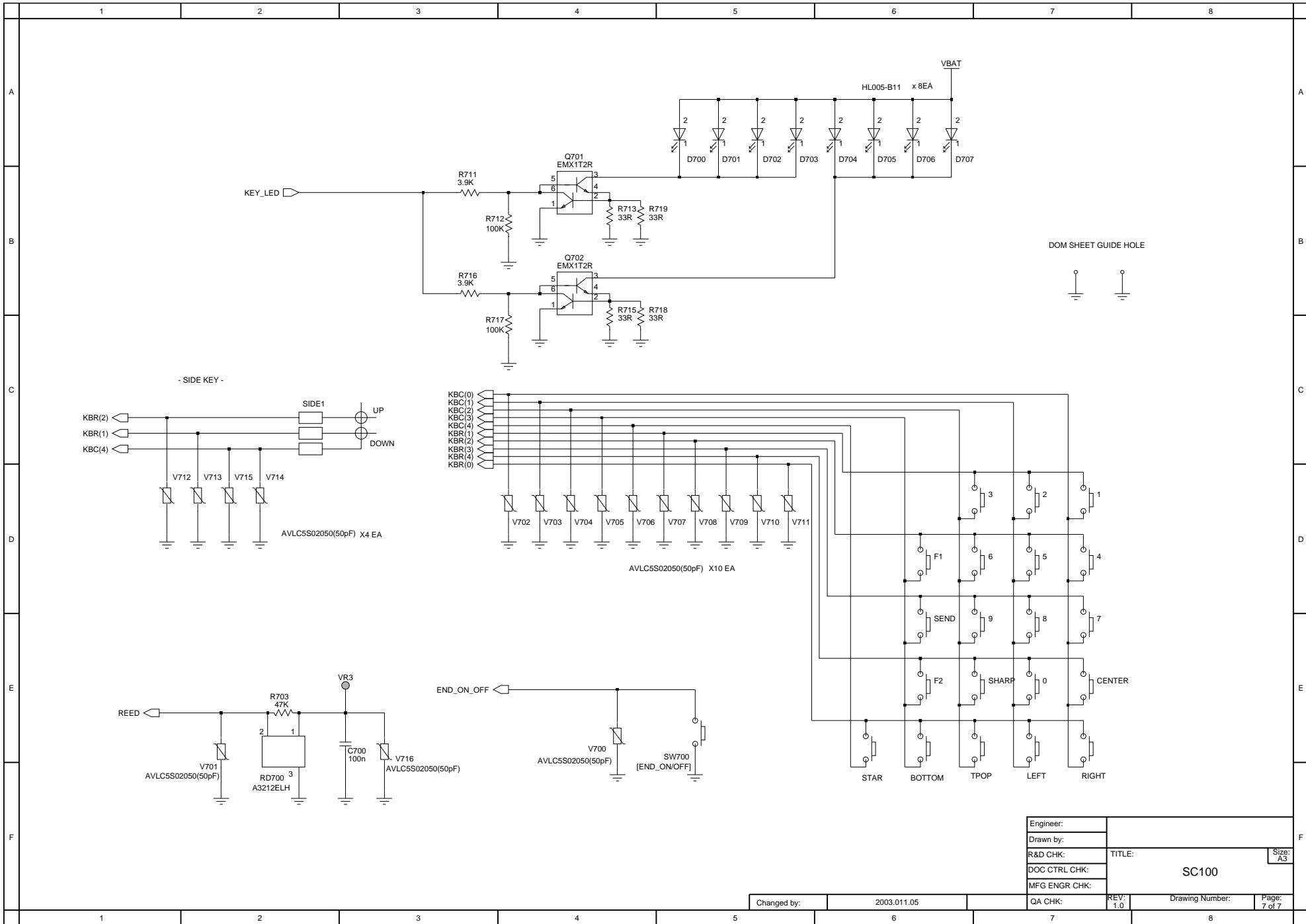


SWITCH-PRESSED = 1.2V
SWITCH-RELEASE = 0.4V
Vref = 1.0V

AVLCS50205(50pF) X2 EA

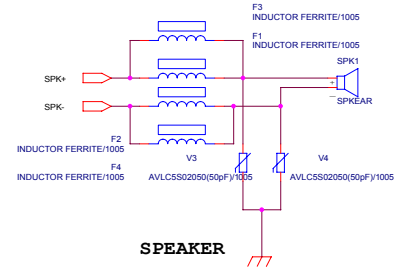
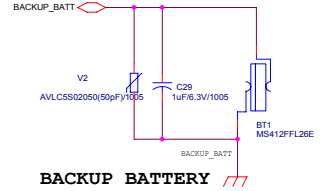
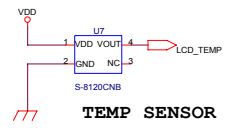
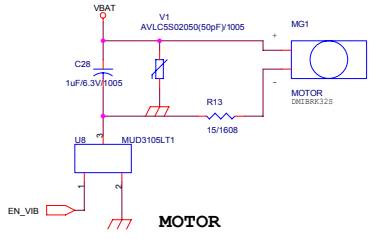
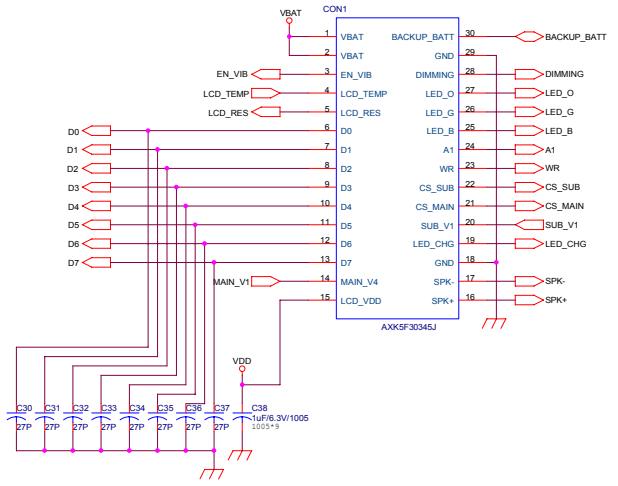
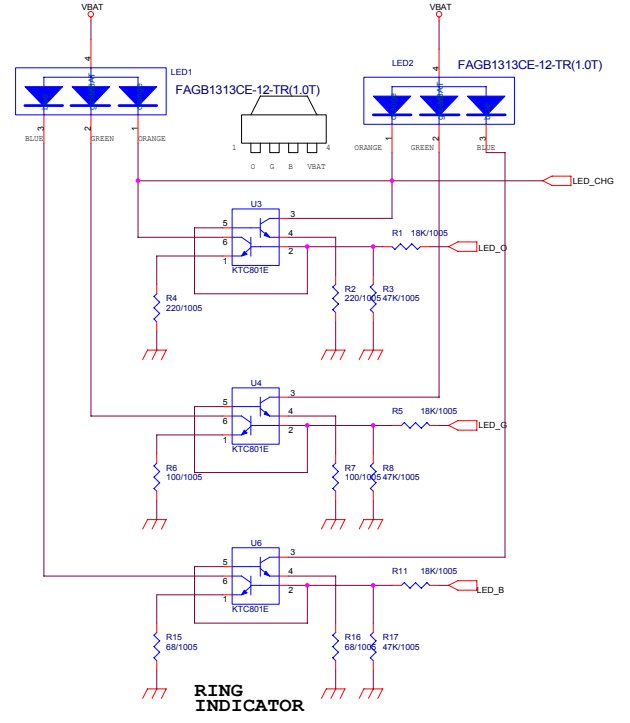
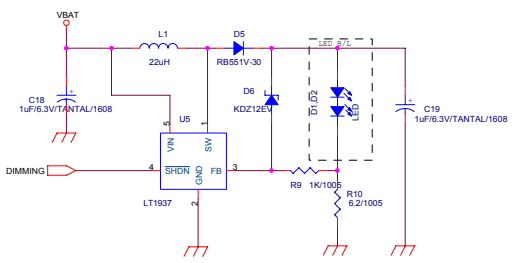
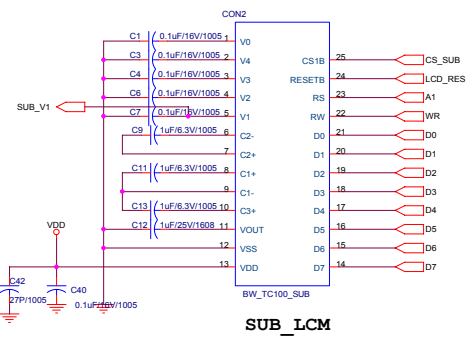
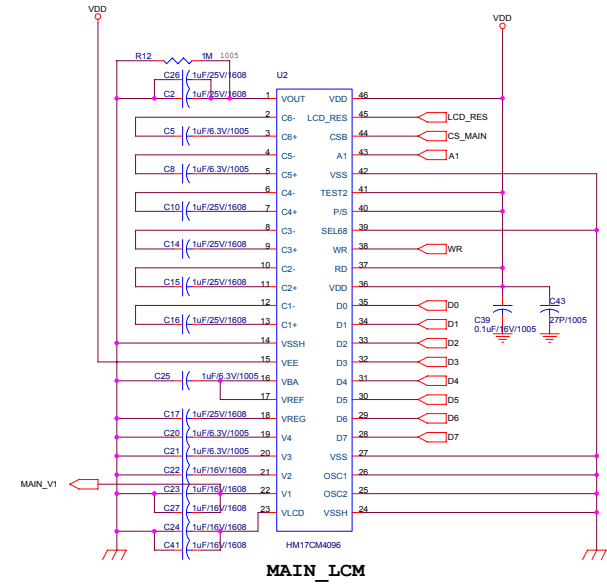
Engineer:	
Drawn by:	
Field OK:	
UCC-e-REL OK:	
TITLE:	SC100
REV:	V3
12 1 8 A	

7.7 Key & Backlight



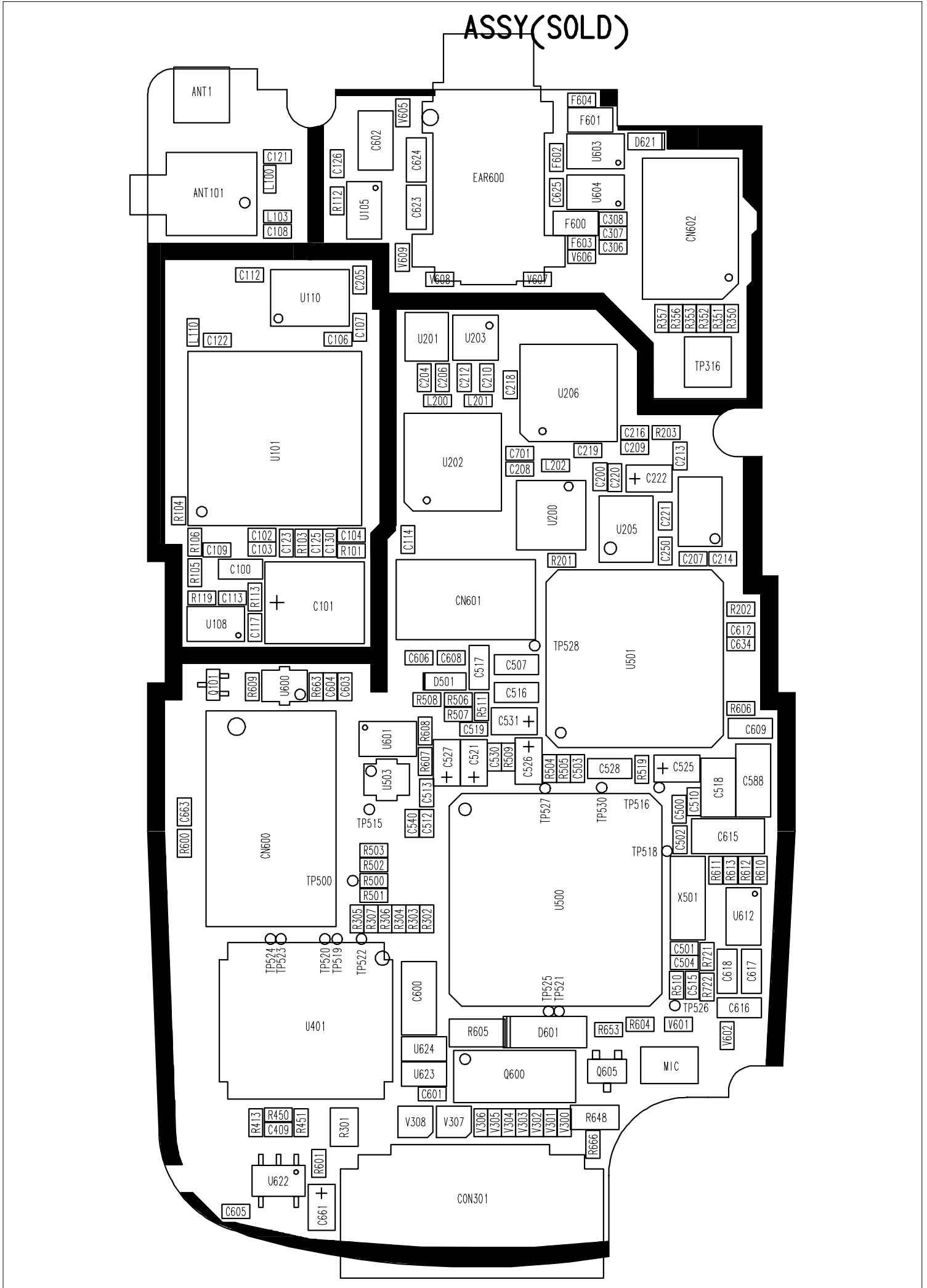
Engineer:	
Drawn by:	
R&D CHK:	TITLE: SC100
DOC CTRL CHK:	
MFG ENGR CHK:	
QA CHK:	REV: 1.0
	Drawing Number:
	Page: 7 of 7

Changed by:	2003.011.05		
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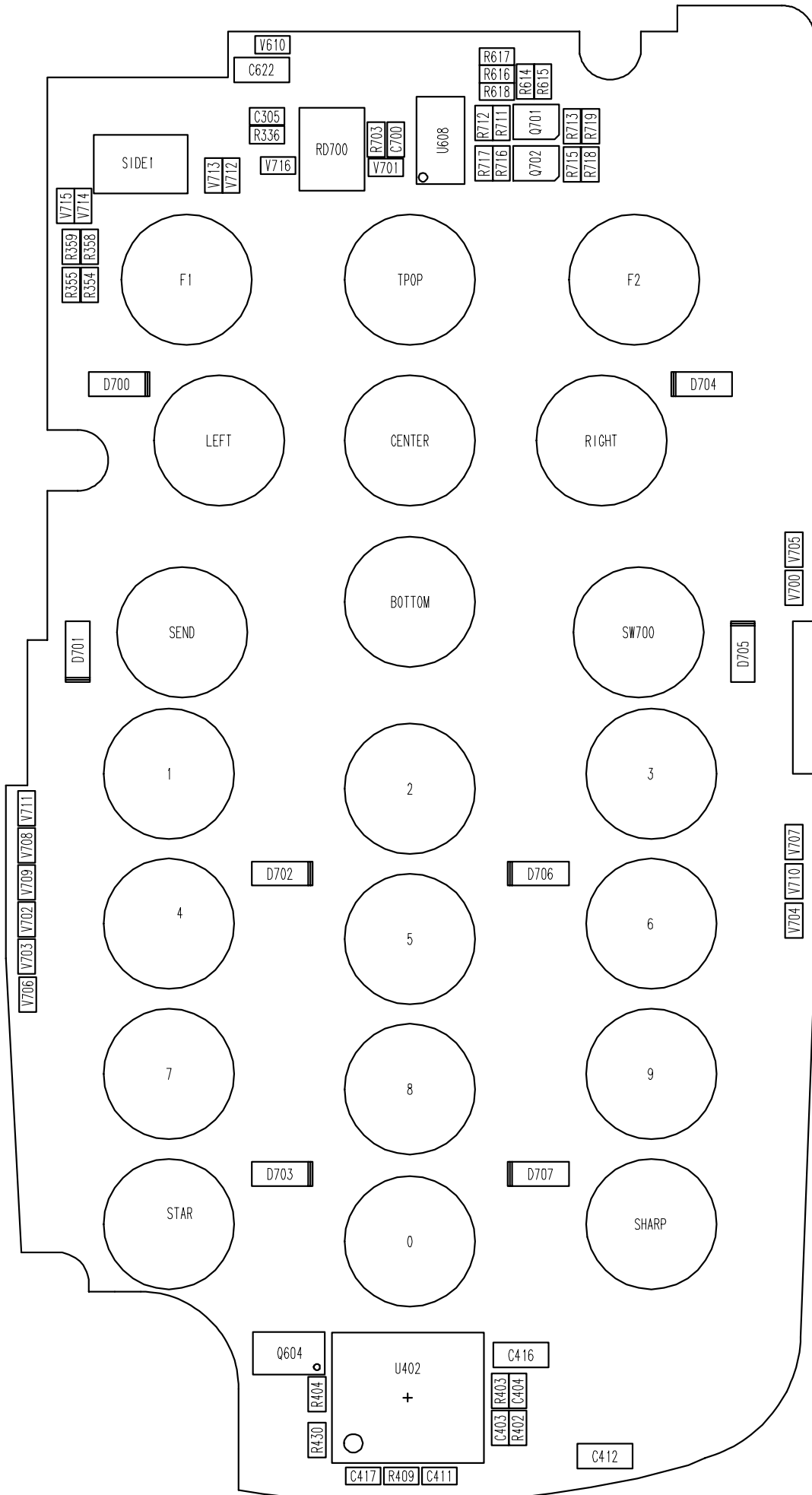
8. PCB Diagram

8.1 Main PCB

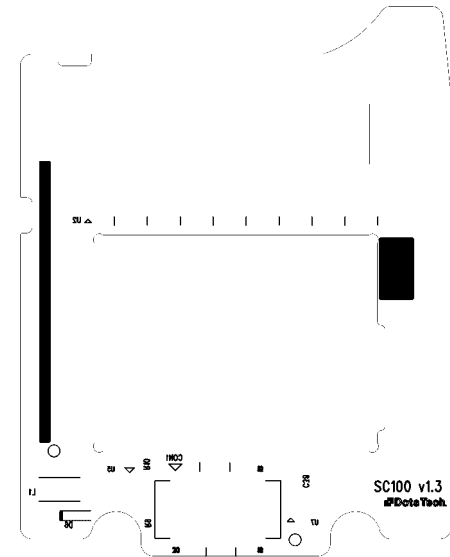
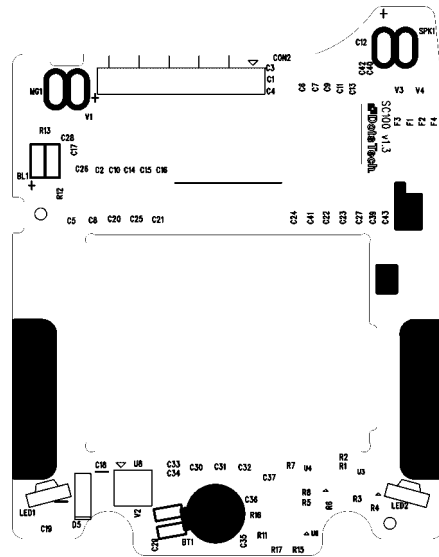


Comment :

ASSY(COMP)



8.2 LCD Module



SC100 v1.3
#DoteTech